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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/765,958	01/18/2001	Bulent Dervisoglu	260/085 US	9164

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EXAMINER	
DOOLEY, MATTHEW C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/765,958	DERVISOGLU ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☑ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,6,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure:

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract is objected to for exceeding 150 words. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 6-7, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel, U.S. 6,408,413, in view of Dervisoglu et al., A Novel Approach for Designing Hierarchal Test Access Controller for Embedded Core Designs in a SoC Environment.

As per claim 1:

Whetsel teaches to a top level circuit block that comprises circuitry analogous to a chip access port controller (Fig.2, Fig.4), as well as plurality of

lower level test control circuit blocks connected to the top level control block, wherein each lower level block comprises circuitry analogous to a SAP controller (Fig.2, Fig.7). However, while Whetsel does teach to upward and downward signal transmission in the hierarchical test structure (Col.4: 20-23, 50-52), it is not expressly taught that the upwardly and downwardly transmitted signals comprise test operation. Dervisoglu expressly teaches to test operation being transmitted upward and downward in a hierarchical test structure (Page 2: line.1-7). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of test operation being transmitted upward and downward in a hierarchical test structure in conjunction with the test system of Whetsel because the combination allows for low level test circuitry to be tested using component level test accessed signals without direct use of pads (Dervisoglu: Page 1: Page 2: lines 11-14).

As per claim 2:

Whetsel teaches to a top level circuit block that comprises circuitry analogous to a chip access port controller (Fig.2, Fig.4), as well as plurality of lower level test control circuit blocks, at least one of which is connected to the top level control block, wherein each lower level block comprises circuitry analogous to a SAP controller (Fig.2, Fig.7). However, while Whetsel does teach to upward and downward signal transmission in a hierarchical test structure (Col.4: 20-23, 50-52), it is not expressly taught that the upwardly and downwardly transmitted signals comprise test operation. Dervisoglu expressly teaches to test operation being transmitted upward and downward between different control circuits

located in various levels of a hierarchical test structure (Page 2: line.1-7). Furthermore, the system of Whetsel allows for the circuitry analogous to a chip access port controller to communicate with the circuit block immediately at a lower level, while also allowing the circuitry analogous to a SAP controller to communicate with the circuit block immediately at a higher level in the hierarchical structure (Fig.2). Finally both Whetsel and Dervisoglu teach to a plurality of test control blocks in a hierarchical structure having a plurality of hierarchical levels (Whetsel Fig.2; Dervisoglu Page 2: line.1-14).

As per claim 6:

The low level test control blocks of Whetsel include test mode select, test data input, and test data output ports (Fig.7).

As per claim 7:

The low level test control blocks of Whetsel include a test access port state controller for controlling the receipt or transmission to or from the test mode select, test data input, and test data output ports (Fig.9A; Col.8: 25-33).

As per claim 11:

The low level test control blocks of Whetsel are functionally identical (Fig.2).

As per claim 12:

The low level test control blocks of Whetsel are structurally identical (Fig.2).

5. Claims 3-5, 8-10, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel, U.S. 6,408,413, in view of Dervisoglu et al., A Novel Approach for Designing Hierarchal Test Access Controller for Embedded Core Designs in a SoC Environment as applied to claim 2 above, and further in view of Muradali et al., U.S. 6,587,981.

As per claim 3:

The combination of Whetsel and Dervisoglu teaches to a hierarchical test control network, however it fails to teach to explicitly teach to a hierarchical tiered structure wherein the low level test control circuit blocks are connected in a serial chain with one of the control circuit blocks at each tier of the hierarchical structure. Muradali teaches to having both a hierarchical tiered structure wherein the low level test control circuit blocks are connected in a serial chain, as well as having one of the low level control circuit blocks at each tier of the hierarchical structure (Fig.2, Fig.3A-3D). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the organizational format provided by Muradali in conjunction with the combined system of Whetsel and Dervisoglu because the tiered system of Muradali gives an efficient design for a hierarchical test system that allows for testing of low level test using component level test accessed signals without direct use of pads, a desired feature already enumerated upon by Dervisoglu.

As per claim 4:

Muradali teaches to having both a hierarchical tiered structure wherein the low level test control circuit blocks are connected in a serial chain, as well as

having one of the low level control circuit blocks connected at any given tier of the hierarchical structure (Fig.2, Fig.3A-3D).

As per claim 5:

The circuitry of Muradali allows for the low level control circuit blocks to be connected to analogous circuitry to a claimed different virtual circuit block for controlling testing thereof (Fig. 3A-3D).

As per claim 8:

The circuitry of Muradali teaches that the low level control circuit blocks connected at the same hierarchical level share a common test mode enable input signal, test reset signal, test mode select signal, and clock signal (Fig.3A-3D).

As per claim 9:

The circuitry of Muradali teaches that the low level control circuit blocks connected at the same hierarchical level output a common test mode data output signal that comprises a logical OR of the test mode data output signals from the low level control circuit blocks connected at the same hierarchical level (Fig.7).

As per claim 10:

The circuitry of Muradali teaches that the low level control circuit blocks connected at the same hierarchical level receives separate test mode data input signals and outputs separate test mode enable output signals to control blocks at an immediately lower level (Fig.3A-3D). Moreover, It has been shown that Dervisoglu teaches to receiving separate test mode data input signals from lower level control blocks at an immediately lower level (Page 2: lines 1-10).

As per claim 13:

The combination of Whetsel, Dervisoglu, and Muradali disclosed above teaches to a hierarchical test control network wherein the low level test control blocks include test mode select, test data input, and test data output ports, and a top level circuit block that comprises circuitry analogous to a chip access port controller, as well as plurality of lower level test control circuit blocks connected to the top level control block (Whetsel Fig.2, Fig.4, Fig.7; Muradali: Fig.3A-3D). Also taught is that the control circuit blocks share a common test mode select signal, test reset signal, and clock signal (Muradali: Fig.3A-3D). Further taught is that the test control blocks at the same hierarchical level, in a chained fashion, receive the second shared test data signal at their second test input port from the control circuit block at the higher tier in the hierarchical structure (Muradali: Fig.3A-3D).

As per claim 14:

The combination of Whetsel and Dervisoglu teach to a top level circuit block that comprises circuitry analogous to a chip access port controller (Whetsel: Fig.2, Fig.4), as well as plurality of lower level test control circuit blocks, at least one of which is connected to the top level control block, wherein each lower level block comprises circuitry analogous to a SAP controller (Whetsel: Fig.2, Fig.7), as well as teaching to test operation being transmitted upward and downward between different control circuits located in various levels of a hierarchical test structure (Dervisoglu: Page 2: line.1-7). Furthermore, the system allows for the circuitry analogous to a chip access port controller to communicate with the circuit block immediately at a lower level, while also allowing the circuitry

analogous to a SAP controller to communicate with the circuit block immediately at a higher level in the hierarchical structure (Whetsel: Fig.2). Finally both Whetsel and Dervisoglu teach to a plurality of test control blocks in a hierarchical structure having a plurality of hierarchical levels (Whetsel Fig.2; Dervisoglu Page 2: line.1-14).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Narayanan et al. U.S. 5,774,474: Fig.3

b. Swoboda U.S. 5,828,824: Fig.3-5

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley at (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 305-3900.

Matthew Dooley
Examiner AU 2133
July 24, 2003

Guy J. Lamarre
for
Albert DeCady
Primary Examiner